Phoebe (RISC PC II)
Functional Specification

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1. Introduction

The functional specification is a detailed specification of the Phoebe (RISC PC II) Project . Phoebe is a development of the existing RISC PC to incorporate as many new developments in the computer world that have occurred since its launch in 1994 e.g. PCI, E-IDE CODECs and SDRAM etc. It is also intended to exploit the performance of the StrongARM processor as much as possible by increasing the speed of the machine from 16 to 64MHz. This specification intends to:

a) Define all software and hardware interfaces (for both internal and external developers)
b) Provide some of the information needed for the Programmers Reference Manual, Technical Reference Manual, DVT and PST
c) Define all the environmental and electrical standards
d) Define the scope of the development

This document includes a product overview followed by a section on each functional area. Where necessary a section will refer to a relevant detailed functional specification. (See section 2.0)

2. Overview

The outline specification of the Phoebe project is described below.

Processor	233Mhz StrongARM on board running at 64MHz I/O
Performance	450k Dhrystones on a monitor supporting 70Hz modes.
Processor expansion card	Interface to support upto 4 x 233Mhz StrongARMs on single processor card) . The card will not form part of this project.
FPA support	*not available*
Floppy drive	Single 2MB unformatted
Hard disc	1 T.B.D. size IDE HD with expansion for a further 3.
CD ROM/DVD ROM	32x slot CD ROM fitted as standard. DVD ROM upgrade possible
Total RAM	SDRAM support only.
DRAM	Expansion upto 512MB of SDRAM with 1 or 2, 32MB SDRAM DIMMs as standard.
ROM	4MB - board layout allocated for up to 8MB.
VRAM	4MB EDO VRAM fitted to board
Video	up to 1024x768 non-interlaced in 32bpp. 1280x1024 24bpp
Drive bays	3 x 5.25”, 1 x 3.5” visible bays, and 2 x 3.5” hidden bays (1 x EIDE drive, CD and 3.5” floppy fitted as standard)
Free Drive Bays	2 x 5.25” visible expansion bays and 1 x 3.5” hidden as standard
PCI interface	4 slots compliant with PCI 2.1 spec (32Mhz 32Bit PCI)
Extended podule slots	Backplane connector similar to RISC PC’s allowing 3 slots
Case type and volume	NLX Mini Tower case, volume = 450x450x190mm (approx.)**.**
Network support	10 and 100 Base-T Ethernet support using a PCI card slot if req.
Parallel port	Enhanced bi-directional multimode parallel port as per RISC PC
Serial ports	2 standard PC-AT style ports and IrDA support. Each will support baud rates up to 460kBaud (the actual performance achieved will depend on software running, user upgrades, screen mode etc.).
ID chip	fitted as per RISC PC
Sound system	16 bit digital CD quality provided by Soundblaster compatible CODEC and VIDC20 sound systems. The Soundblaster sound and Acorn sound are mixed with CD/DVD output
Line input/output	Stereo 3.5mm jack sockets on rear
Microphone input	Mono 3.5mm jack socket on front of case
Internal speakers	Mono
Headphone output	Fitted on front, inserting headphone switches off speakers
Joystick	15 way D-type standard PC game port for dual joystick support
MIDI support	MIDI input and output at rate of 31.25K baud on game port
PSU	230W NLX standard PSU

For comparison:

RISC PC700:	ARM710, 50k Dhrystones in MODE 0, up to 2 IDE devices, 2MB floppy disc, 4,8 or 16MB RAM, 10,1,2MB VRAM, 800×600×32b video, 4 single Podule slots, Ethernet network card replacing one single Podule slot, bi-directional parallel port, serial port, headphone socket

The upgrade will offer in the region of 150-200% of the performance of a StrongARM RISC PC

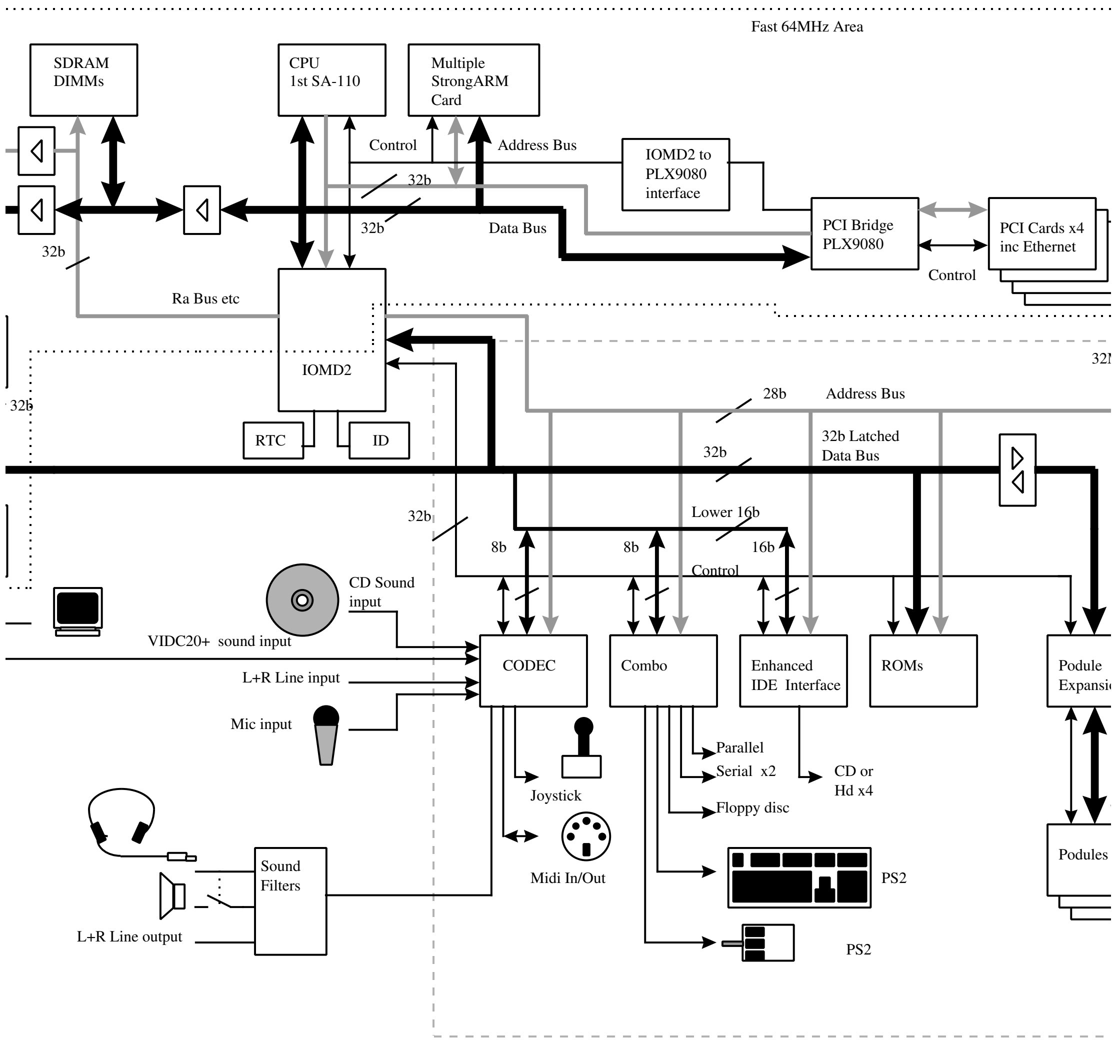

Figure 1. Phoebe system block diagram

2.1

2.2 Overview of software development

The objective of the operating system development is to extend RISC OS 3.7 to be more compliant with the StrongARM processor and its potential multiprocessor applications within Phoebe. There is a requirement to provide an improved version of the basic desktop environment and improve the existing product. Phoebe requires a revised IOMD and VIDC20 to achieve these objectives and hence the software must be designed to be compatible with these revisions.

The delivered operating system will be in the form of sources and images. Some sources may be suitable for assembly for older platforms than Phoebe, however, the images will be suitable only for the Phoebe platform, and no testing will be done by the project on the suitability for earlier platforms.

The software parts of the Phoebe project will be delivered to the user on ROM and hard disc. The operating system, some basic applications and fonts will be provided in ROM, the remainder on hard disc.

It is not expected that the introduction of new features into the operating system will cause the failure of software written to be compliant with previous style guides.

Some faults found in RISC OS 3.7 have been identified and will be fixed by the Phoebe Software.

2.3 Outline of development testing strategy

Reviews are being held, and will continue to be held, that cover all aspects of the project. Design verification is assured by a series of reviews which cover all aspects of the project. The functional specifications are being reviewed, and various reviews will be held during implementation. These are noted on the project plan. Reviews are made up from peers, relevant people from outside the team, and sometimes an external expert.

2.3.1 Hardware

In addition to the reviews, the product will be put through the usual hardware quality assurance process, and tested against the environmental requirements and standards given later in this document. The software faults database and software testing process will also be used to trap hardware faults.

2.3.2 Software

Design reviews and code walkthroughs of software will be held, along with specific documentation reviews. White box test programs for areas being developed will be written to prove the initial functionality of the modules.. Black box test programs will be produced prior to machines being available in line with functional specs. The whole system will be audited in line with all other Acorn products, providing a functional and stable operating system.

2.4 External dependencies

Major external dependencies in priority order:

a) IOMDII+ (Chandler)
b) PCI Bridge IC from PLX Tech (PCI9080)
c) VIDC20 shrink
d) Continuation of VRAM Technology

2.5 Compatibility

Phoebe will not be designed with the sole intention of being backwards compatible with applications developed for earlier generations of Acorn computers. However programs may work in a single processor mode.

2.5.1 Summary

a) *The design should only require small modification to be backwards compatible , if any.*

3. Project deliverables

The project will deliver the following:-

a) Phoebe Machine as per overview section 3.0
b) Manuals as per section 9.0
c) Revised Software ROMs and Disc image
d) Packaging
e) Test specification and software

4. Functional Description

4.1 Introduction

The following sections describe the basic functionality of Phoebe. Where further detailed descriptions are required there will be a reference to the relevant Acorn Specification or 3rd party data sheet for the corresponding device.

4.2 CPU and RAM

EC-QPWLC-TE	Digital Semiconductor SA-110 Microprocessor Technical Reference Manual

Phoebe will use a 233MHz StrongARM IC (or greater) fitted on a daughter card for upgradeability, running at a bus clock of 64MHz.
It will support up to 516MB divided into two 256MB SDRAM DIMMs and 4MB EDO VRAM both supplied as standard). The execution space available for each application is limited to 28MB, although it can access all the memory for data, should this be required.

The StrongARM will operate in an asynchronous enhanced mode with a 32bit configuration. Within this configuration, the ARM will almost always be running in 26-bit modes, as most of RISC OS (and all current user programs) will not run in 32-bit modes. Any FIQ-driven device code will be entered in 32-bit mode, and so may have to be modified.

The video system will use EDO VRAM as its display memory. Using EDO VRAM means that high bandwidth screen modes will not affect the machine‘s speed. The video system will only have a single 4M EDO VRAM fitted to the PCB. EDO VRAM which is not being used for the display will be automatically made available for ordinary program use, but only to a 1MB granularity. The user will not notice this happening.

4.2.1 Summary:

a) DRAM (32or 64MB SDRAM as 2 DIMMs with expansion upto 512MBs)
b) Video memory fixed at 4MB EDO VRAM
c) 233Mhz StrongARM Processor CPU with 32KB cache (16K data and 16K address, on-chip memory manager and write buffer)
d) 3V3 Powered subsystem (VRAM will be 5V)

4.3 Additional Processor Expansion

There will be two expansion routes on the main 64MHz processor bus, each will be allowed to act as local bus master. Control between each processor will be via a combination of 3 bus requests, 3 bus grants and 3 wait signals. Priority between processors may be assigned in a fixed or round robin system. The possible expansion cards are described below, each will require a copy of the standard StrongARM expansion card within their design. Neither form part of this project :-

4.4 ROM

The operating system will be provided initially in two 42 pin DIL packages giving 4MB or 8MB (via jumper settings) of operating system image. These will be socketed to allow for further user upgrading later. The ROM's specified will be 120ns with a page burst of 50ns. This allows an access speed of upto 8.33MHz and a page access of upto 20MHz - RISC PC ROMs are currently clocked at 5.33MHz.

The ROMs are connected in the system diagram on the 32MHz I/O world bus rather than the 64MHz fast processor bus. This is because the ROMs would not gain from the speed increase as they are inherently slower than the 16Mhz bus currently used. The ROMs will be +5V operation.

IOMDII will support up to two 16MB banks of ROM with individually controllable timing parameters. These are configured as two adjacent areas of 4M x 32 bit Read Only Memory the required one being selected by the physical address line La<24>. Although the area operates as a contiguous 32MB whole, the access timings for each area can be set independently, and are variable from around 220ns downwards in steps of 31.25ns. In addition, support is provided for burst mode ROMs which allow rapid access to sequential addresses controlled by La<2> and La<3>.

In Phoebe only one bank of ROM is used (Bank 0). The motherboard will have two 1M x 16 bit ROM sockets fitted (expandable to 2M x 16 bit via jumpers) providing up to 16MB of ROM space per bank. Two fast page mode 1M x 16bit ROMs will be fitted initially. IOMDII provides two five bit registers to control the individual timing parameters; one for each bank. Three bits control the basic access speed, and two bits control whether burst is used and if so, the burst access speed.

4.4.1 Summary:

a) 4MB OS ROM fitted initially running at X.XXMHz
b) Potential upgrade to two 16MB banks in existing hardware
c) +5V ROM operation.

4.5 IOMDII

IOMDII (Chandler) is a new memory and I/O controller chip developed for Phoebe. It is designed to work with StrongARM in both single and multiple processor operations, allowing upto 3 separate local bus masters using a modified version of the open bus system. The intercommunication between multiple processors will be achieved by using an internal SRAM area with binary semaphores and circular lists.

The memory and processor bus will run at a 64Mhz speed, the I/O bus will run at 32Mhz. Both will be 32 bit wide. IOMDII's memory interface will work with SDRAM, and VRAM memory in the same system. The I/O system will have a generic interface that will connect to the ROM, Combo, CODEC and Podule interfaces. IOMDII's memory and processor interface will interface to a PCI bridge via an EPLD (for control only) and allow the PCI bridge to run upto 64Mhz, It will also have direct support to the VIDC video controller.

IOMDII contains eight general purpose I/O DMA channels, one sound DMA channel, one cursor DMA channel and one video DMA channel. The general purpose DMA channels may be used for the CODEC, hard drive, parallel port, podule bus and PCI bus interfaces.

Refer to the IOMDII functional specification for full information.

4.5.1 Summary:

a) High speed direct interface to StrongARM (64Hz)
b) SRAM area dedicated to the interfacing between multiple ARM processors
c) Support for 2 x SDRAM DIMMs (4 DRAM banks)
d) Control of VRAM, including generation of transfer cycles and a DMA channel
e) Generic I/O bus to interface to ROM and Combo IC etc.
f) Most of the functionality of IOMD, including interrupt masking, counter timers etc.
g) Eight general purpose I/O DMA channels and 3 dedicated DMA channels
h) Video data can be obtained from SDRAM or VRAM

IOMDII is being developed by Acorn using VHDL

4.6 Video

The video controller will be a revised version of VIDC20, reducing the silicon from a 1 micron process down to a 0.6 micron process. This will give a 100% performance increase over the existing VIDC20 product. This will enable higher resolution and greater pixel depth than VIDC20.

The new revised "Shrunk" VIDC20 should allow a video system to run with a bandwidth of 400Mbytes using upto a possible 50Mhz VRAM input clock rate and a 64 bit bus, with pixel clock upto 150MHz or above (200Mhz would be required to attain the 1600x1200 screen mode). The basic system maximum is to aim for 1024x768 in 32 bits per pixel using a 4M VRAM system and 1360 x1024 in 16 bits per pixel using a peak allowable bandwidth of 320Mbytes/sec. A possible 1600x1200 may be attained in 16bpp.

See section 9 for pin out information on the screen interface.

4.6.1 Summary:

a) New 0.6um VIDC20 150 to 200Mhz pixel clock
b) 4M VRAM with VRAM interface upto 50Mhz
c) *Screen resolution of 1024x768 in 32 bits per pixel or greater*

4.7 Sound System and CODEC interface

AD1816 Analog Semiconductor Single Chip Audio System

The sound system on phoebe will be supplied by two devices; the existing VIDC20 16 bit sound coupled with a CODEC chip. Refer to section 9 for all pin out information.

4.7.1 Audio

The VIDC20 sound system will provide 16 bit CD quality sound output via an I^2S interface and a serial DAC. This sound will be merged with the sound inputs and output from the CODEC as well as the internal CD ROM sound output. The CODEC has a Soundblaster compatible register set allowing PC sound to be created rather than simulated. The CODEC will support 2 DMA channels for sound in/out and output.

The CODEC gives a stereo line input and output interface to Phoebe for hi-fi quality I/O, along with a microphone input and internal CD audio sound input.

All sound will be 16 bit CD quality audio and will be controlled by volume up/down/mute buttons.

4.7.2 Expansion

One header will be provided for waveblaster expansion of the CODEC system. This will allow an interface to a MIDI interpreter, synthesiser engine and effects processor along with access to standard MIDI samples including various instruments and percussive sounds.

4.7.3 Joystick interface

A 15 way D-type PC game port will be provided for Phoebe by the CODEC IC. This will support two analogue joystick interfaces.

4.7.4 MIDI Interface

The CODEC also provides an MPU-401 compatible MIDI I/O interface running at a rate of 31.25K baud. It is connected via the 15 way D-type PC style game port. In order to interface directly to MIDI equipment a small amount of external circuitry will be required, this is however the same as all IBM PC compatible MIDI interfaces.

4.7.5 Summary

a) 16 bit digital Soundblaster compatible sound system
b) Stereo line Input and Output
c) Microphone Input
d) Headphone Output
e) Joystick interface
f) MIDI Input and Output
g) Volume controls
h) Expansion for waveblaster cards
i) Expansion for a DSP serial audio data port

4.8 Floppy

FDC37C67X	SMC Enhanced Super I/O Controller with Fast IR

The hardware combo chip (SMC's FDC37C67X) has the same interface as the SMC FDC37C665 used on the RISC PC. The floppy disc interface hardware is integrated into the SMC (Standard Microsystems Corporation) FDC37C67X super I/O Controller device. This device contains a floppy disc controller which is software and register compatible with the Intel 82077, and utilises a '765 disc controller core. For a detailed description refer to SMC's datasheet "FDC37C67X - Super I/O Controller", and the RISC PC floppy drive functional Spec 0197,264/FS (the same signals are available on the FDC37C67X as on the 37C665)

The floppy disc interface connector is the normal 0.1" pitch, 2-row, 34-way box header (Acorn reference number 0803,102).

The power supply for the floppy drive will be a standard 4 pin device(see 0197,000/FS RISC PC Functional Specification for further details)

It is recommended that the cable length between the 34-way interface connector and the disc drive should not exceed 300mm (as per RISC PC).

4.8.1 Summary:

a) 3.5" 2MB Floppy drive as per the RISC PC

4.9 Hard disc and CD ROM/DVD ROM

The main components of the IDE system hardware are; 4 bi-directional data bus buffers, a PAL containing the IDE address decode logic to create the buffer enable signals and DMA controls , and a pair of 40-way IDE interface connectors.

The system will be "ATA-2" / "Enhanced IDE" compliant with a data transfer rate of 16.6Mb capable of PIO mode 4 transfers and possibly DMA mode 2. The system will contain two master/slave pairs allowing upto 4 devices. The devices that may be used are either IDE or ATAPI compliant, hence CD ROM and DVD ROM may be connected. The design differs considerably from the RISC PC in that It is controlled via a PAL device designed in house rather than a COMBO chip. Each master/slave pair is buffered separately and connected to the peripherals via a cable with two 40 way IDC interface connectors.

The interface will support one DMA channel per master/slave pair.

The unit will be fitted with one Slot type 32x CD ROM and one T.B.D. M E-IDE hard disc as standard.

The IDE interface connectors are the normal 0.1" pitch, 2 row, 40-way box headers (Acorn ref.: 0803,103).

The power supply for the hard discs will be a standard 4 way connector (see 0197,000/FS RISC PC Functional Specification for further details)

The Sizes of Hard Disc and speed of the CD ROM supported are not confirmed.

4.9.1 Summary:

a) Upto 16.6MB transfer rate.
b) upto 4 device support
c) ATAPI compliant interface for CD and potential DVD support
d) Enhanced IDE/ATA-2 compliant PIO Mode 4 operation or DMA mode 2

4.10 Keyboard and mouse

FDC37C67X SMC Enhanced Super I/O Controller with Fast IR

The keyboard and mouse interfaces will both be IBM PC (PS/2 6 pin mini DIN connector) compatible. Both interfaces will be controlled by the Combo IC. Refer to section 9 for pin out information.

4.11 Parallel

FDC37C67X SMC Enhanced Super I/O Controller with Fast IR

The parallel interface will be provided through the SMC FDC37C67X combo chip. This provides hardware handshaking and FIFO giving a minimum speed better than XXK characters per second.

4.11.1 Hardware Configuration

The hardware configuration will be very similar to that of the RISC PC but using IOMDII and the FDC37C67X (refer to 0197,258/FS RISC PC Parallel Hardware Functional Specification and The SMC specification for the FDC37C67X Super I/O controller.

See section 9 for pin out information.

4.12 Serial

FDC37C67X SMC Enhanced Super I/O Controller with Fast IR

Phoebe will be designed to have two serial ports, however in addition to this there will be IrDA RX and TX signals allowing Infra Red communications. The second serial port may be used at the same time as the IrDA port. The serial port hardware is configurable up to a 460KBaud, but this may not be achievable under the desktop- the speed of which will depend on the screen mode in use, other applications etc. The FDC37C67X I/O chip has two high speed UARTs and 16 byte FIFO's to improve speed of interface. It also contains control circuitry for Modems.

The following new Baud rates will be provided:

a) 230,400
b) 460,800

4.12.1 Hardware Configuration

The serial port interface hardware is integrated into the Combo IC. This device contains all the necessary hardware and control registers for the serial port with the exception of the interrupt control. All inputs and outputs have EMI filtering and voltage level converters.

Both serial ports will have the same pin out and functionality as the single RISC PC port apart from the increased baud rates. For further information refer to the following specifications , 0197,259/FS RISC PC Serial Hardware Functional Specification and the SMC specification for the FDC37C67X Super I/O controller.

See section 9 for pin out information.

4.13 Expansion interfaces

4.13.1 PCI Interface

The PCI interface will be implemented using the following major components :- IOMDII, PLX9080, a PCI bridge controller designed to interface between PCI and the Intel i960 I/O controller IC, a custom designed EPLD to interface between the i960 interface and IOMDII, and a PAL to create the arbitration logic across the 4 PCI slots.

The interface logic will fit into the architecture on the 64Mhz open bus, this allows for the possible increase in speed to the 64MHz PCI specification when it becomes available, further to this it allows the system to use the full 132 MB bandwidth of the 32Mhz 32 bit PCI system

The NLX mini tower case will provide 4 PCI slots through the rear of the case, using the riser card.

The interface will conform to PCI functional Specification 2.1. Refer to this document for a more detailed description of the interface itself.

4.13.2 Podule Interface

The Podule interface will conform to the Acorn Expansion Card Specification (Acorn part number 0472,200), formerly Podule Electrical Specification. The Extended Acorn Expansion Bus maintains full backward compatibility with the original expansion bus.

The interface will be connected to the 32MHz I/O bus from IOMDII. The signals from IOMDII will have to be modified to interface to the Podule bus. This will be achieved by using a small PAL to bridge between the two.

There will be 3 Podule slots available via a podule backplane in the same manner as the RISC PC. They will be accessed via the rear of the case through 3 punch out holes.

4.14 Power management

The power supply will be a standard 230W NLX specified PSU (part no. EN-8235941 from Enlight Corp. conforming to both FCC and CE) with the following power rails :-

Power rail	Tolerance	Current rating
+3.3V	4%	14A
+5V	5%	22A
-5V	5%	.5A
5VSB	5%	1A
+12V	5%	6A
-12V	5%	0.8A

4.14.1 Power budget

The table below gives an estimate of the power budget for Phoebe, assuming the following configuration; SDRAM SIMM, 2xEDO RAM SIMM, VRAM SIMM, 3xEIDE drives, CD ROM, floppy , 2x PCI cards, and 2x podules.

Part	3.3V (A)	3.3V (W)	5.0V (A)	5V (W)	12V (A)	12V (W)	-12V (A)	-12V (W)	Total Power (W)
Main PCB	3.3	10.0	2.0	10.0			0.25	3.00	23.0
Floppy			2.0	10.0	0.75	9.0			19.0
Hard Disc (per disc)			0.5	2.5	0.50	6.0			(3 off) 25.5
CD/DVD ROM			0.4	2.0	0.80	9.6			11.6
PCI (per card)			5.0	25.0	0.5	6.0			(2 off) 62.0
Podule			1.0	5.0	0.25	3.00			(2 off) 16.0
Total Power (W)			20.9	104.5	4.45	54.6	.25	3.00	162.1

The power budget estimate for the main PCB includes 0.25A for the keyboard supply, 0.1A for the mouse supply, 0.8A for the DIMM module , and allowance in the -12v supply for the provision of a regulated -5v supply to the podule backplane. The 5V supply is regulated down to 2V for the StrongARM core.

5. Mechanical

5.1 Enclosure

The Phoebe case conforms to the NLX motherboard specification release 1.2 © Intel Corp. March 1997. The design allows the motherboard to be replaced simply by removing the bottom of the case. In removing this panel the motherboard is unplugged from a riser card. This riser card has all the connections to the peripherals in the case. The floppy, hard drives, all front panel switches, PCI cards and PSU are connected to the riser. Thus the motherboard can be removed with the minimum of cable disconnections.

The case is a Mini tower design, with the following expansion interfaces :-

3 x 5.25" visible bays (CD's etc)
1 x 3.5" visible bay (floppy drive etc)
2 x 3.5" hidden bays (hard drives etc)

4 PCI slots at rear of case (cards connect to Riser)
3 Podule slots at rear of case (cards connect to backplane card)

Overall dimensions approximately 450mm x 450mm x190mm.

Access to the internals of the case is via removable sides and base. All panels are connected with easily removable clips. The Visible bays are accessed by removing the front panel of the case.

5.2 Packaging

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Refer to the above specification for details of the packaging style.

Products will be shipped in fully enclosed cardboard based packaging which can be recycled. Provision should be made to enable point of sale sleeves to be added at a later date, as required.

The packaging will be sufficiently robust to complete the following transportation cycle twice - from the manufacturing site to warehouse, to distributor/dealer on to customer and back to repair centre. During this cycle the system will arrive undamaged.

The package will be easy to produce from flat-pack.

The package will be appropriately marked with following as a minimum:

a) Model number, product code and description
b) "CE" markings
c) Barcode label
d) Recyclable packaging symbol
e) Pack symbols i.e. this way up arrows, etc.
f) Opening instructions

The package will be simple for the user to open.

6. Conditions of Use

6.1 Reliability

A typically hard worked machine might see the following usage pattern:

a) expected lifetime 7 years
b) 220 working days per year
c) 8 hours active use per day
d) 7 switch on/off cycles per day

With the above duty cycle, a MTBF of 25,000 hours is to be achieved.

To achieve this operational life routine cleaning by the user and economic servicing and repair may be necessary.

The target failure rate is zero.

External connectors, apart from keyboard and mouse, will have an insertion/extraction cycle of 50 times minimum. The keyboard and mouse will exceed 200 cycles.

Acorn will continue to provide spare parts support for Phoebe for five years from the date of its last manufacture.

With the additional conditions:

Floppy duty cycle (% of POH)

10% Motor on
90% Motor off

The Customer can expect no greater than the following failure rates:

Year after delivery	%Units failing
1st year	2%
2nd year	2%

The customer can expect no “dead on arrivals”.

For details of MTBF for individual components refer to the specification for that item.

6.2 Safety

The product will be designed and certified to EN60950 for Europe, CSA 22.2 No.950 and UL1950 for USA and Canada, and AS3260 for Australia and New Zealand. It will therefore display the ‘CE’ mark as conforming to the Low Voltage Directive (LVD).

6.3 EMC

6.3.1 Interference Generation

From the date of first production, the product shall be tested and certified to EN55022 -Class B, 'Radiated and conducted emissions. The product shall thus be able to display the "CE" mark as conforming to the EMC directive.

Further approvals that may be required are:-

Australia and New Zealand	CISPR 22 (This is equivalent to EN55022)
Canada and USA	FCC Rules Part 15 - Class B (CFR47 Part15)

6.3.2 Interference Susceptibility

From the date of first production output the product will be certified to EN50082-1.

6.4 Environmental

6.4.1 Operating

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The units must continue to operate under the same conditions as specified for the existing RISC PC.

6.4.2 Non-operating but unpackaged

The units must not be damaged under the same conditions as specified for the existing RISC PC.

6.4.3 Shipment and storage

The units must not be damaged under the same conditions as specified for the existing RISC PC.

7. Manuals

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The table below details the manuals that will be supplied by the Phoebe project

Type	Title	Pages	Colours	Style
End User manuals	Phoebe Welcome Guide	XXX	1	Book
	RISC OS XXXX User / Apps Guide	XXX	1	HTML
Hardware Manuals	Technical Reference Manual	XX+drgs	1	A4 ring bound
	Service Manual	XX + drgs	1	Phcopy
Programmer's Manual?	Programmer‘s Reference Manual	XXX	1	Book ?
Other Documents	Owner Registration Card			
	Release Note			
	Documentation for upgrades			

8. Service and support

The product will be guaranteed against defects in manufacture for a period of one year from date of sale to the end user. The product should be capable of supporting a three year extended guarantee period.
In the UK all machines will be sold with an on-site warranty, allowing for a visit by an engineer within 24 hours of end user call. All defective modules will be returned for replacement to the original manufacturing site.

Telephone support will also be provided on all machines sold within the UK. This support will be available during office hours on normal working days.

9. Expansion Interfaces

9.1 Standard Interfaces

The following external interfaces are connected directly to the main PCB and exit the box at the bottom rear of the machine.

9.1.1 Monitor Port

The monitor port is a standard 15 pin high density D socket as below

Pin	Signal Name	Notes
1	RED	
2	GREEN	
3	BLUE	
4	N/C	
5-8	GND	
9	+5v	Acorn Specific Signal
10	GND	
11	ID[0]	
12	+12v	Acorn Specific Signal
13	H/C SYNC	C Sync option is acorn specific
14	V/C SYNC	C Sync option is acorn specific
15	N/C	

The following signal ratings apply

RGB	Source Impedance	75 Ohms
	Signal Level	0 to 0.7v positive into 75 ohms
Horizontal/ Composite (OR)Sync	Source Impedance	75 Ohms
	Signal Level	5v typ. into open circuit (Exceeds minimum TTL thresholds into 1K)
Horizontal/ Composite (OR)Sync	Source Impedance	75 Ohms
	Signal Level	5v typ. into open circuit (Exceeds minimum TTL thresholds into 1K)
ID[0] * - 4k7 pull up to +5V	High	> 2.0v
* note ID[3:1] not supported	Low	< 0.8v
5v feed for TV (SCART control via external series resistor)	Maximum current rating	75mA
	Fuse protection	0.8A
+12v (feed for SCART function switch control)	source Impedance	1K
	Voltage Output	11.25 Typ. Into open circuit

9.1.2 Keyboard Interface

The keyboard 6 pin mini DIN PS2 port is connected as below

Pin	signal name	Description
1	KDATA	KDATA Open drain with pull-up. Data signal synchronised with KCLK
2	NC2	Not connected
3	0V	OV Supply Filtered
4	Vsupp	5 volt supply filtered and fused at 2A.Maximum permissible current drain 300mA.
5	KCLK	Open drain with pull-up. Clock synchronising data transfer between keyboard and host system, generated by the keyboard.
6	NC6	Not connected

9.1.3 Mouse interface

The mouse 6 way mini DIN PS2 is connected as below

Pin	signal name	Description
1	MSDATA	Mouse DATA Open drain with pull-up. Data signal synchronised with KCLK
2	NC2	Not connected
3	0V	OV Supply Filtered
4	Vsupp	5 volt supply filtered and fused at 2A.Maximum permissible current drain 300mA.
5	MSCLK	Open drain with pull-up. Clock synchronising data transfer between Mouse and host system, generated by the mouse.
6	NC6	Not connected

9.1.4 Serial Ports 1 and 2

The 9 way D-type male connectors are defined as below:-

Pin	Signal Name	Direction	Function
1	DCD	Input	Data Carrier Detect
2	/RXD	Input	Receive Data
3	/TXD	Output	Transmit Data
4	DTR	Output	Data Terminal Ready
5	0v		Signal Ground
6	DSR	Input	Data Set Ready
7	RTS	Output	Request to send
8	CTS	Input	Clear to Send
9	RI	Input	Ring Indicate

9.1.5 Game port interface

The Pin outs for the Game port 15 way D-type on the motherboard are as below

Pin	Signal Name	Direction	Function
1	+5V	Output	PSU Current limited to 200mA
2	JAB1	Input	Switch input for Joystick A
3	JACX	Input	X Co-ordinate for Joystick A
4	0V	Output	Ground
5	0V	Output	Ground
6	JACY	Input	Y Co-ordinate for Joystick A
7	JAB2	Input	Switch input for Joystick A
8	+5V	Output	PSU Current limited to 200mA
9	+5V	Output	PSU Current limited to 200mA
10	JBB1	Input	Switch input for Joystick B
11	JBCX	Input	X Co-ordinate for Joystick A
12	MIDI_OUT	Output	Sends serial MIDI data out
13	JBCY	Input	Y Co-ordinate for Joystick A
14	JBB2	Input	Switch input for Joystick B
15	MIDI_IN	Input	Receives serial MIDI data in

9.1.6 Parallel Port

The 25 way D-type female connector is defined as below:-

Pin	Signal	Type	Active	Function in Printer Mode
1	/STROBE	OPD	LOW	Indicates that the data at the parallel port is valid.
2-9	PD0-7	I/O		'port data' Bi-directional data bus. Configured as output
10	/ACK	IP	LOW	Acknowledge. Indicates that data has been received.
11	BUSY	IP	HIGH	Indicates that the printer cannot accept additional data.
12	PE	IP	HIGH	Paper End Indicates that that the printer is out of paper.
13	SCLT	IP	HIGH	Select Indicates that the printer is selected
14	/AUTOFD	ODP	LOW	Automatic Feed Causes the printer to automatically add one line
15	/ERROR	IP	LOW	Indicates the printer has an error condition
16	/INIT	ODP	LOW	Initialises (Resets) the printer
17	/SLCTIN	OPD	LOW	Select Input. Selects the printer
18-25	0V			Ground

I = TTL compatible input
O = Output
D = Open drain
P = 4K7 pull-up to VCC

9.1.7 Line Input and Output

This will be a standard 3.5mm stereo jack socket. The interface will be nominally 1Vrms centred around 2.1 (Vref).

9.2 Front Panel Interfaces

The following ports are connected on the front of the case, in addition to the On/off button, reset button, volume up and down buttons and the infra red panel.

9.2.1 Headphone Socket

This will be a standard 3.5mm stereo jack socket. The interface will be nominally 1Vrms centred around 2.1 (Vref).

9.2.2 Microphone input

This is a standard 3.5mm mono jack socket. The interface will be nominally 1Vrms centred around 2.1 (Vref)

10. Change History

Issue A	6th December 1996	Initial specification
Issue B	29th May 1997	Second draft, revised layout and more detail
Issue C	8th February 1998	Fitting into NLX mini tower case with 230W PSU
Issue D	4th March 1998	more detail and updates
Issue E	11th March 1998	tidy up of typos and release for developers only